

2-14-05

2182

# TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

In re application of:	Enrique Musoll; Adolfo M. Nemirovsky; Mario D. Nemirovsky; Narendra Sankar
Serial No.:	09/602279
Filed:	06/23/00
Docket:	MIPS.0168-00-US
For:	METHODS AND APPARATUS FOR BACKGROUND MEMORY MANAGEMENT

Attached hereto is Form PTO-1449 listing documents believed relevant to the subject application. It is respectfully requested that the Examiner review the information disclosed herein in detail, independently evaluate each item carefully in the consideration of the pending claims and return an initialed copy of each form to the undersigned.

This disclosure statement should not be construed as a representation that a search has been made, that no other material information as defined in 37 C.F.R. § 1.56(a) exists, or as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b) or is available as a reference under 35 U.S.C. § 102 *et seq.* Applicant reserves the right to swear behind or otherwise disprove the alleged "prior" nature of any art cited should the facts support and the situation warrant such an action.

It is believed that this disclosure complies with the requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98, and the Manual of Patent Examining Procedures § 609. If for some reason the examiner considers otherwise, it is respectfully requested that the undersigned be called so that any deficiencies can be remedied.

A copy of each document is enclosed. Some of the documents may have markings thereon. No significance is intended to be attached to the markings.

Respectfully submitted,

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Date: 1-31-05

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	09/602279
				Filing Date	06/23/00
				First Named Inventor	Enrique Musoll Adolfo M. Nemirovsky Mario D. Nemirovsky Narendra Sankar
				Group Art Unit	2182
				Examiner Name	Tammara R. Peyton
Sheet	1	of	3	Attorney Docket Number	MIPS.0168-00-US

**U.S. PATENT DOCUMENTS**

Examiner Initials	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup>			
	AA	5708814		Short et al	01/13/1998	
	AB	5724565		Dubey et al	03/03/1998	
	AC	6460105		Jones et al	10/01/2002	
	AD	6523109		Stephan G. Meier	02/18/2003	
	AE	6535905		Kalafatis et al	03/18/2003	
	AF	2001/0004755		Levy et al	06/21/2001	
	AG	2001/0043610		Nemirovsky et al	11/22/2001	
	AH	2001/0052053		Nemirovsky et al	12/13/2001	
	AI	2002/0016883		Musoll et al	02/07/2002	
	AJ	2002/0049964		Takayama et al	04/25/2002	
	AK	2002/0071393		Enrique Musoll	06/13/2002	
	AL	2002/0083173		Musoll et al	06-27-2002	
	AM	09/608750		Nemirovsky et al	Not published	

**FOREIGN PATENT DOCUMENTS**

Examiner Initials	Cite No. <sup>1</sup>	Foreign Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number <sup>4</sup>	Kind Code <sup>5</sup>			
	BA	WO 03/005645		Sampath et al	06/25/2002	

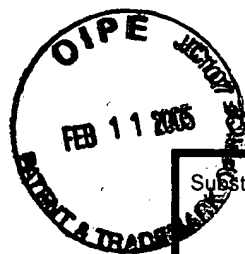
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<sup>2</sup>Unique citation designation number. <sup>3</sup>See attached Kinds of U.S. Patent Documents. <sup>4</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3).

<sup>5</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>6</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>7</sup>Applicant is to place a check mark here if English language Translation is attached.

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<b>Substitute for form 1449A/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
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				Examiner Name	Tammara R. Peyton
Sheet	2	of	3	Attorney Docket Number	MIPS.0168-00-US

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>	
	CA	MELVIN ET AL, "Extended Instruction Set for a Packet Processing Applications:, July 5, 2001, Disclosure Document #496559, USPTO		
	CB	MUSOLL ET AL, "Hardware Algorithm for Allocating and De-Allocating Consecutive Blocks of Memory, " April 3, 2001, Disclosure Document #491557, USPTO		
	CC	MUSOLL ET AL, "Mechanism to Overflow Packets to a Software Controlled Memory When They Do Not Fit intoa Hardware Controlled Memory, July 3, 2001, Disclosure Document #496391, USPTO		
	CD	MUSOLL ET AL, "Mechanism for Allowing a Limited Packet Head and/or Tail Growth Without Moving the Packet to a Different Memory Location," April 16, 2001, Disclosure Document #492429, USPTO		
	CE	MUSOLL ET AL, "Mechanism to Activate a Context When No Stream is Running in a Multi-Streaming Processing Core", April 16, 2001, Disclosure Document #492431, USPTO		
	CF	MUSOLL, ENRIQUE, "Functional Validation of a Packet Management Unit:, May 18, 2001, Disclosure Document #429011, USPTO		
	CG	SAMPATH ET AL, "Mechanism To Un-Speculatively Pre-Fetch Instructions From the Thread Associated to a Packet:, July 5, 2001, Disclosure Document #491527, USPTO		
	CH	YAMAMOTO, WAYNE. <i>An Analysis of Multistreamed, Superscalar Processor Architectures</i> . University of California Santa Barbara Dissertation. December 1995. Santa Barbara, US.		
	CI	YAMAMOTO et al. "Increasing Superscalar Performance Through Multistreaming." <i>Parallel Architectures and Compilation Techniques (PACT '95)</i> . 1995		
	CJ	The PowerPC Architecture: A Specification for a New Family of RISC Processors. 2 <sup>nd</sup> Ed. May 1994. pp. 70-72. Morgan Kaufmann. San Francisco, US.		
	CK	MC68020 32-Bit Microprocessor User's Manual. 3 <sup>rd</sup> Ed.. 1989. pp. 3-125, 3-126, and 3-127. Prentice Hall, NJ, US.		

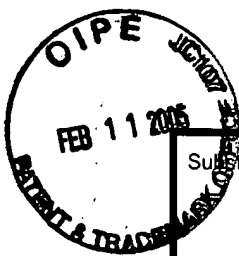
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